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1	BRS	L1	277	"control register" near3 mask	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/03 16:26	
2	BRS	L2	2	1 SAME "control value"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/03 16:28	
3	BRS	L3	77	1 SAME " value"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/03 16:29	
4	BRS	L4	9	3 and "initial value"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/03 16:29	
5	BRS	L5	8	4 not 2	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/03 16:29	

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1 The 8 by 8 display 83
R. F. Sproull , I. Sutherland , A. Thomson , S. Gupta , C. Minter
ACM Transactions on Graphics (TOG) January 1983
Volume 2 Issue 1

2 A microprogramming language for the B-1726 82
D. J. DeWitt , M. S. Schlansker , D. E. Atkins
Conference record of the 6th annual workshop on Microprogramming September 1973
The "New Products" section of a recent issue of COMPUTER I carried announcements of four new commercial computers offering writeable microprogram memory. Three of these, the HP2100S, the Interdata Model 85, and the Microdata 3200, provide at least rudimentary facilities to develop trailored instruction sets, special algorithms, or entire applications functions. The fourth was the IBM System/370, Model 115. In addition, the two-level microprogrammed Nanodata ...

3 Low contention semaphores and ready lists 80
Peter J. Denning , T. Don Dennis , Jeffrey A. Brumfield
Communications of the ACM October 1981
Volume 24 Issue 10
A method for reducing semaphore and ready-list contention in multiprocessor operating systems is described. Its correctness is established. Its performance is compared with conventional implementations. A ready list implemented as a ring network is proposed and evaluated.

4 TWIST-TOP: transputers with I-stores test out processor 80
George S. Davidson
Proceedings of the 1990 ACM annual conference on Cooperation January 1990
Future parallel computing systems will require high speed communication, efficient synchronization primitives, and low overhead context switches for communicating and synchronizing instruction streams. These issues are developed with respect to I-storage, a global memory that can synchronize requests for data values issued before the data is produced. Methods to implement these I-stores are described for the transputer architecture, with programs and timing results. This description, for bo ...

5 High-performance raster graphics for microcomputer systems 77
Andreas Bechtolsheim , Forest Baskett
ACM SIGGRAPH Computer Graphics , Proceedings of the 7th annual conference on Computer graphics and interactive techniques July 1980
Volume 14 Issue 3
A frame buffer architecture is presented that reduces the overhead of frame buffer updating by three means. First, the bit-map memory is (x,y) addressable, whereby a string of pixels can be accessed in parallel. Second, the pixel-change operation is performed by hardware in a single read-modify-write cycle. Third, multiple objects in the frame buffer are addressable simultaneously by a set of address registers. The remaining task of generating (x,y) addresses and providing new data can be m ...

6 Warp architecture and implementation 77
M. Annaratone , E. Arnould , T. Gross , H. T. Kung , M. S. Lam
ACM SIGARCH Computer Architecture News , Proceedings of the 13th annual international symposium on Computer architecture June 1986
Volume 14 Issue 2
This paper describes the scan line array processor (SLAP), a new architecture designed for high-performance yet low-cost image computation. A SLAP is a SIMD linear array of processors, and hence is easy to build and scales well with VLSI technology; yet appropriate special features and programming techniques make it efficient for a surprisingly wide variety of low and medium level computer vision tasks. We describe the basic SLAP concept and some of its variants, discuss a particular planne ...

7 Variable-length capabilities as a solution to the small-object problem 77
Edward F. Gehringer
Proceedings of the seventh ACM symposium on Operating systems principles December 1979
A capability system which supports very small objects can achieve flexible and efficient protection. This paper presents a scheme for representing both large and small entitles In a computation, down to integers and character strings, as objects. This is achieved by a generalization of tagged memory to encompass extended data types; and by the use of variable-length capabilities, which can be very short if they are close to the object they reference. As developed here, the design assumes a ...

8 Modulo scheduling: Modulo schedule buffers 77
Matthew C. Merten , Wen-mei W. Hwu
Proceedings of the 34th annual ACM/IEEE international symposium on Microarchitecture December 2001
As VLIW/EPIC processors are increasingly used in real-time, signal-processing, and embedded applications, the importance of minimizing code size and reducing power is growing. This paper describes a new architectural mechanism, called the Modulo Schedule Buffers, that provides an elegant interface for the execution of modulo scheduled loops. While the performance is similar to that of kernel-only modulo scheduling, this mechanism has a number of advantages, including minimal code expansion. Rath ...

9 Design of the real-time executive for the Univac(r) 418 system 77
John Michael Williams
Proceedings of the 1966 21st national conference January 1966
The UNIVAC 418 system hardware The 418 is a small- to medium-scale real-time computer announced to the general public in September of 1964. It is available in two models, identical except for storage speed (two or four microseconds). Storage and registers

10 Hardware/software tradeoffs in a variable word width, variable queue length buffer memory 77
A. C. Parker , A. W. Nagle
ACM SIGARCH Computer Architecture News , Proceedings of the 4th annual symposium on Computer architecture March 1977
Volume 5 Issue 7

This paper describes a buffer memory design which is integratable on a single 40 pin package. The memory consists of four variable word width, variable length queues, address logic, and logic for configuring the data widths and queue lengths. Simple program commands input on the data lines reconfigure the memories when the circuit is in program mode. In data mode, WRITE and READ requests to a particular buffer enable the memory to load and access itself, update its pointers, and check for f ...

11 Considerations for new tactical computer systems 77

Jon C. Strauss , Kenneth J. Thurber

ACM SIGARCH Computer Architecture News , Proceedings of the 4th annual symposium on Computer architecture March 1977

Volume 5 Issue 7

The real-time command and control environments characteristic of tactical military systems and industrial process control systems place unique and conflicting design requirements on a support computer system. These requirements include fast context switching, selective protection of programs and their files, controlled sharing of program and files, high processing speed, flexible, yet fast priority structure for interrupts and program execution, flexible high-speed I/O and flexible intercom ...

12 The Datasaab FCPU microprogramming language 77

Harold W. Lawson , Lars Blomberg

ACM SIGPLAN Notices , Proceedings of the meeting on SIGPLAN/SIGMICRO interface May 1973

Volume 9 Issue 8

This paper describes the high level microprogramming language (ML) used in microprogramming the FCPU (Flexible Central Processing Unit) developed by the Datasaab sector of Saab-Scania AB. The background of the use of machine dependent high level languages is discussed. The global structure and microinstruction organization of the FCPU are presented. The structure of the ML and microprograms are introduced followed by an example of the use of ML. A summary of the syntactical structure of FCP ...

13 Virtual machines: ReVirt: enabling intrusion analysis through virtual-machine logging and replay 77

George W. Dunlap , Samuel T. King , Sukru Cinar , Murtaza A. Basrai , Peter M. Chen

ACM SIGOPS Operating Systems Review December 2002

Volume 36 Issue SI

Current system loggers have two problems: they depend on the integrity of the operating system being logged, and they do not save sufficient information to replay and analyze attacks that include any non-deterministic events. ReVirt removes the dependency on the target operating system by moving it into a virtual machine and logging below the virtual machine. This allows ReVirt to replay the system's execution before, during, and after an intruder compromises the system, even if the intruder rep ...

14 A control strategy for small computer systems 77

Harold W Lawson

Proceedings of the 8th annual workshop on Microprogramming September 1975

A general purpose hardware oriented control structure is presented. This outer control structure can be used to implement a variety of target languages. Further, the control structure can be adapted to a variety of Large Scale Integration components including general purpose ALU's microprogram storage medias and programmable logic arrays. The independence from specific components reduces the binding ...

15 MU6-G, a new design to achieve mainframe performance from a mini-sized computer 77

D. B.G. Edwards , A. E. Knowles , J. V. Woods

Proceedings of the 7th annual symposium on Computer Architecture May 1980

MU6-G is a high performance machine useful for general or scientific applications. Its order code and architecture are designed to be sympathetic to the needs of the operating system and to both the compilation and execution of programs written in high level languages and to support a word size suitable for high precision scientific computations. Advanced technology, coupled with simplicity of design, is used to achieve a high and more readily predictable performance. Innovative features in ...

16 Towards an efficient, machine-independent language for microprogramming 77

David A. Patterson , Karl Lew , Richard Tuck

Proceedings of the 12th annual workshop on Microprogramming November 1979

A machine independent low level language YALLL is presented. This language produces microcode for two very different machines: Hewlett Packard HP 300 and Digital Equipment Corporation VAX 11/780. The efficiency of this language is tested by comparing two examples on both machines to microassembly coded versions. To our best knowledge, this is the first time programs have been compiled and executed on two different microarchitectures. These examples also let us compare the efficiency of the ...

17 The big three - today's 16-bit microprocessor 77

R. K. Bell , W. D. Bell , T. C. Cooper , T. K. McFarland

Proceedings of the 13th annual workshop on Microprogramming November 1980

This paper reports on the functional evaluation of the three 16-bit microprocessors, namely the Intel 8086, the Zilog Z8000, and the Motorola MC68000. These microprocessors were employed in several CRT applications, both monochrome and color. Execution time benchmark tests were made, mechanization problems compared and instruction/architectural characteristics highlighted. Conclusions and recommendations are made applicable to terminals and similar Sperry Univac products.

18 Design of a user-microprogrammable building block 77

Michael Kraley , Randall Rettberg , Philip Herman , Robert Bressler , Anthony Lake

Proceedings of the 13th annual workshop on Microprogramming November 1980

A user-microprogrammable computer has been developed for use as a building block in general-purpose and dedicated computer systems. The architecture is designed to be easily microprogrammed and features a 32-bit, vertically oriented microinstruction. The processor has a 135-nanosecond cycle time, either 16- or 20-bit macro data paths, and 1024 hardware registers. A significant fraction of the processor bandwidth may be budgeted for I/O processing to allow the substitution of microcode for e ...

19 Real-time software engineering in Ada: observations and recommendations 77

M. Borger , M. Klein , R. Veltre

Proceedings of the conference on Tri-Ada '89: Ada technology in context: application, development, and deployment January 1989

20 A proposed high-speed computer design 77

Trevor Turton

ACM SIGARCH Computer Architecture News October 1979

Volume 7 Issue 10

The designs of several high performance general purpose computers built during the last two decades are examined. The performance limitations they encountered and their approaches to overcoming these problems are discussed. An alternate design approach is described which avoids these problems. This is to have the computer support the simultaneous execution of several independent programs by multiprogramming its various components at the sub-instruction level. Estimates of its performance are mad ...

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